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<u>L50</u>	15 and l46	3307	<u>L50</u>
<u>L49</u>	4206503.pn.	1	<u>L49</u>
<u>L48</u>	(l34 or l36 or l38) and (task\$4 or thread\$3 or loop\$4 or branch\$4)	2	<u>L48</u>
<u>L47</u>	L46 and l44	27	<u>L47</u>
<u>L46</u>	(712/230-248) [CCLS]	3307	<u>L46</u>
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
<u>L45</u>	((multipl\$5 or alu\$1 or arithmetic\$3 or adder\$1 or subtract\$3) near25 general near1 purpose near1 register\$1 and (threaded or thread\$1 or threading)) near55 branch\$4	0	<u>L45</u>
<u>L44</u>	L43 and branch\$3	216	<u>L44</u>
((multipl\$5 or alu\$1 or arithmetic\$3 or adder\$1 or subtract\$3) near25 general			

<u>L43</u>	near1 purpose near1 register\$1 and (threaded or thread\$1 or threading))	281	<u>L43</u>
<u>L42</u>	L41 not l40	8	<u>L42</u>
<u>L41</u>	((multipl\$5 or alu\$1 or arithmetic\$3 or adder\$1 or subtract\$3) near25 general near1 purpose near1 register\$1 near55 (threaded or thread\$1 or threading))	51	<u>L41</u>
<u>L40</u>	L39 and branch\$5	43	<u>L40</u>
<u>L39</u>	((multipl\$5 or alu\$1 or arithmetic\$3 or adder\$1 or subtract\$3) near15 general near1 purpose near1 register\$1 near45 (threaded or thread\$1 or threading))	49	<u>L39</u>
<u>L38</u>	5640538.pn. and (threaded or thread\$1 or threading)	0	<u>L38</u>
<u>L37</u>	L36 and (threaded or thread\$1 or threading)	0	<u>L37</u>
<u>L36</u>	5724563.pn.	2	<u>L36</u>
<u>L35</u>	L34 and (threaded or thread\$1 or threading)	0	<u>L35</u>
<u>L34</u>	6275508.pn.	2	<u>L34</u>
<u>L33</u>	4454595.pn. and (task\$3 or thread\$3 or process\$4 or loop\$4 or branch\$5)	2	<u>L33</u>
<u>L32</u>	(alu\$1 or arithmetic\$3 or adder\$1 or subtract\$3) near15 general near1 purpose near1 register\$1 near25 (threaded or thread\$1 or threading)	1	<u>L32</u>
<u>L31</u>	L24 and l12	3	<u>L31</u>
<u>L30</u>	L24 and l11	3	<u>L30</u>
<u>L29</u>	L24 and l9	39	<u>L29</u>
<u>L28</u>	L24 and l8	139	<u>L28</u>
<u>L27</u>	L24 and l7	36	<u>L27</u>
<u>L26</u>	L24 and l6	142	<u>L26</u>
<u>L25</u>	L24 and l5	219	<u>L25</u>
<u>L24</u>	L23 and (analog\$5) and digital	5933	<u>L24</u>
<u>L23</u>	L22 and (one or single or "on") near3 chip	16782	<u>L23</u>
<u>L22</u>	(mux or multiplex\$4 or select\$5 or crossbar\$1 or rout\$4) near12 (fpga or pld\$1 or array\$1 or pla\$1)	187704	<u>L22</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L21</u>	l10 and l12	11	<u>L21</u>
<u>L20</u>	l10 and l11	17	<u>L20</u>
<u>L19</u>	l10 and l9	22	<u>L19</u>
<u>L18</u>	l10 and l8	133	<u>L18</u>
<u>L17</u>	l10 and l7	47	<u>L17</u>
<u>L16</u>	l10 and l6	126	<u>L16</u>
<u>L15</u>	l10 and l5	241	<u>L15</u>
<u>L14</u>	l10 and l4	4909	<u>L14</u>
<u>L13</u>	(718/106-108)![CCLS]	1429	<u>L13</u>
<u>L12</u>	(718/106-108)[CCLS]	1429	<u>L12</u>
<u>L11</u>	(709/220-222)[CCLS]	3813	<u>L11</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L10</u>	l4 and context\$1	4909	<u>L10</u>
<i>DB=PGPB,USPT; PLUR=YES; OP=OR</i>			
<u>L9</u>	(716/15,16)![CCLS]	890	<u>L9</u>

<u>L8</u>	(716/2-17)![CCLS]	9037	<u>L8</u>
<u>L7</u>	(710/305-317)[CCLS]	5286	<u>L7</u>
<u>L6</u>	(712/2-39, 225,227, 228)[CCLS]	4694	<u>L6</u>
<u>L5</u>	(712/2-300)[CCLS]	12871	<u>L5</u>
<i>DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L4</u>	L3 and (one or single or "on") near3 chip	15634	<u>L4</u>
<u>L3</u>	L2 and (mux or multiplex\$4 or select\$5 or crossbar\$1 or rout\$4)	120591	<u>L3</u>
<u>L2</u>	L1 and (analog\$5) and digital and (cell\$1 or array\$1 or element\$1 or block\$1)	128551	<u>L2</u>
<u>L1</u>	(reconfigur\$5 or configur\$5 or programmab\$5 or programab\$5) and (fpga or pld\$1 or array\$1 or pla\$1)	984597	<u>L1</u>

END OF SEARCH HISTORY